REMARKS

This application has been carefully reviewed in light of the Office Action dated August 25, 2008. Claims 1, 4, 7, 8 and 9 are in the application, with Claim 1 being independent. Claims 1, 4, 7 and 9 have been amended herein. Reconsideration and further examination are respectfully requested.

The title of the invention was objected to as allegedly not being descriptive. The title has been amended herein, as suggested by the Examiner. Withdrawal of this objection is respectfully requested.

Claims 1 to 4 and 7 to 9 were rejected under 35 U.S.C. § 103(a) over U.S. Patent No. 4,065,809 (Matsumoto) in view of U.S. Patent No. 5,214,775 (Yabushita). Reconsideration and withdrawal of the rejections is respectfully requested, as explained in further detail below.

Amended independent Claim 1 is directed to a processor system comprising a single semiconductor substrate on which is provided a built-in processor, a memory controller, an external bus interface, a processor bus, and a cross-bar switch. The external bus interface is connected to an external processor from outside of the single semiconductor substrate. The processor bus is connected with the built-in processor and the external bus interface. The cross-bar switch mutually connects the memory controller and the processor bus. The cross-bar switch comprises at least a first port connected to the memory controller and a second port connected to the processor bus. First and second signal lines for inputting first and second enable signals are connected to reset lines of the built-in processor and the external bus interface, respectively. The first enable signal is asserted while the second enable signal is deasserted, so that the built-in processor is in a

reset state to suppress issuance of a request for using the processor bus from the built-in processor and the external processor connected to the external bus interface can use the processor bus and the second port of the cross-bar switch exclusively. The second enable signal is asserted while the first enable signal is deasserted, so that the external bus interface is in a reset state to suppress issuance of a request for using the processor bus from the external processor connected to the external bus interface and the built-in processor can use the processor bus and the second port of the cross-bar switch exclusively.

The applied references, even if properly combined, are not seen to disclose or suggest the subject matter of Claim 1.

In particular, none of Matsumoto and Yabushita are seen to disclose at least the claimed features of (i) the first enable signal being asserted while the second enable signal is deasserted so that the built-in processor is in a reset state to suppress issuance of a request for using the processor bus from the built-in processor and the external processor connected to the external bus interface can use the processor bus and the second port of the cross-bar switch exclusively and (ii) the second enable signal being asserted while the first enable signal is deasserted so that the external bus interface is in a reset state to suppress issuance of a request for using the processor bus from the external processor connected to the external bus interface and the built-in processor can use the processor bus and the second port of the cross-bar switch exclusively.

As understood by Applicant, Matsumoto merely describes a system including a CPUa 11 and a CPUb 12, where the CPUa 11 is prevented from producing a read-write signal R/Wa 26 by setting the logic level for the signal WAITa 25 to "1" and the CPUb is similarly prevented from producing an independent read-write signal R/Wb 44 by

setting the logic level for the signal WAITb 41 to "1". Matsumoto, column 4, lines 56 to 63, column 6, lines 42 to 48, and Figure 1. Matsumoto is not seen to disclose an external bus interface, much less one having a reset state to suppress requests from the external processor connected to the external bus interface to use the processor bus.

In contrast, Claim 1 recites an external bus interface in a reset state to suppress issuance of a request from the external processor connected to the external bus interface to use the processor bus, when a second enable signal is asserted and a first enable signal is deasserted, so that the built-in processor uses the processor bus and the second port of the cross-bar switch exclusively. Claim 1 further recites a built-in processor in a reset state to suppress issuance of a request from the built-in processor to use the processor bus, when a first enable signal is asserted and a second enable signal is deasserted, so that the external processor connected to the external bus interface can use the processor bus and the second port of the cross-bar switch exclusively.

Accordingly, Matsumoto is not understood to disclose or suggest at least (i) the first enable signal being asserted while the second enable signal is deasserted so that the built-in processor is in a reset state to suppress issuance of a request for using the processor bus from the built-in processor and the external processor connected to the external bus interface can use the processor bus and the second port of the cross-bar switch exclusively and (ii) the second enable signal being asserted while the first enable signal is deasserted so that the external bus interface is in a reset state to suppress issuance of a request for using the processor bus from the external processor connected to the external bus interface and the built-in processor can use the processor bus and the second port of the cross-bar switch exclusively.

Yabushita has been studied, but is not seen to overcome the deficiencies of Matsumoto. Therefore, even when Matsumoto and Yabushita are considered in the proposed combinations, assuming that such could permissibly be combined, the resulting combination would not have disclosed or suggested all of the features of Claim 1.

Accordingly, it is respectfully submitted that Claim 1 recites subject matter that would not have been obvious from any permissible combination of the applied art, and allowance of Claim 1 is respectfully requested.

The other claims in the application are each dependent from the independent claim and are believed to be allowable over the applied references for at least the same reasons. Because each dependent claim is deemed to define an additional aspect of the invention, however, the individual consideration of each on its own merits is respectively requested.

An Information Disclosure Statement was filed on December 10, 2008. Consideration of the art cited therein is respectfully requested.

The application is believed to be in condition for allowance, and a Notice of Allowance is respectfully requested.

Applicant's undersigned attorney may be reached in our Costa Mesa, California office by telephone at (714) 540-8700. All correspondence should be directed to our address given below.

Respectfully submitted,

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